Claims

1. A semiconductor memory apparatus (14), comprising an integrated semiconductor memory (18) and a connecting apparatus (16), with

the connecting apparatus (16) comprising:

- a large number of contacts (20) which are arranged like a matrix and by means of which the semiconductor memory apparatus (14) can be connected to a printed circuit board device (12) for signaling purposes, with the large number of contacts (20) comprising a first contact group (K1) whose connections cannot be varied, a second contact group (K2) whose connections can be varied, and an allocation contact for receiving an external allocation signal; and

the integrated semiconductor memory (18) comprising:

- a large number of internal connections (22), with the large number of internal connections (22) comprising a first group (I) of internal connections (22) whose connections are associated with contacts (20) in the first contact group (K1) of the connecting apparatus and are connected to them for signaling purposes, and a second group (II) of internal connections (22) whose connections can be connected to different contacts (20) in the second contact group (K2) of the connecting apparatus (16) for signaling purposes,

- an allocation connection (30) which is connected to the allocation contact (44) of the connecting apparatus (16) for signaling purposes;

- a signal producing device (32, 52) which is connected to the allocation connection (30) for signaling purposes and is designed to produce an internal allocation signal (M_int; M1_int, M2_int) which can assume at least two different states, depending on the external allocation signal which is received via the allocation contact (44),

- an allocation device (30), which is arranged between the second group (II) of internal connections (22) and the second contact group (K2) of the connecting apparatus (16) and is connected to them and to the signal producing device (32; 52) for signaling purposes, with the allocation device (30) being designed to carry out an allocation process between the internal connections (22) in the second group (II) and the contacts (20) in the second contact group (K2) of the connecting apparatus (16) by producing electrical signal connections between them as a function of the internal allocation signal (M_int; M1_int, M2_int) which is produced by the signal producing device (32; 52).

2. The semiconductor memory apparatus (14) as claimed in claim 1, in which

- the integrated semiconductor memory (18) also comprises a large number of external connections (24) which are connected to the contacts (20) in the connecting apparatus (16) in a nonvariable manner for signaling purposes,
- the internal connections (22) in the first group of internal connections are connected to the respective external connections (24) for signaling purposes, and
- the internal connections (22) in the second group of internal connections can be connected via the allocation device (30) to the respective external connections (24) for signaling purposes.

3. The semiconductor memory apparatus (14) as claimed in claim 2, in which the large number of external connections (24) are arranged in at least one row, preferably essentially centrally, on the integrated semiconductor memory (18).

4. The semiconductor memory apparatus (14) as claimed in one of the preceding claims, in which the second group (II) of internal connections (22) comprises connections to which access is intended to be made quickly, preferably addressing connections and/or command connections.

5. The semiconductor memory apparatus (14) as claimed in one of the preceding claims, with the signal producing device (32; 52) being designed to produce an internal allocation signal (M_int) with two different states, in which

- when the internal allocation signal (M_int) assumes the first state, the connections of the contacts (20) in the second contact group (K2) of the connecting apparatus (16) assume a first connection state which can be predetermined, and
- when the internal allocation signal (M_int) assumes the second state, the connections of the contacts (20) in the second contact group (K2) of the connecting apparatus (16) correspond essentially to the first connections, reflected along the longitudinal center axis or transverse center axis of the semiconductor memory apparatus (14).

6. The semiconductor memory apparatus (14) as claimed in claim 5, in which the signal producing device (32; 52) is designed to produce an internal allocation signal (M1_int, M2_int) with three different states, and when the internal allocation signal (M1_int, M2_int) assumes the third state, the connections of the contacts (20) in the second contact group (K2) of the connecting apparatus (16) correspond essentially to the first connections, reflected along the other center axis of the semiconductor memory apparatus (14) as in the second state.

7. The semiconductor memory apparatus (14) as claimed in claim 6, in which the signal producing device (32; 52) is designed to produce an internal allocation signal (M1_int, M2_int, M3_int) with four different states, and when the internal allocation signal (M1_int, M2_int, M3_int) assumes the fourth state, the connections of the contacts (20) in the second contact group (K2) of the connecting apparatus (16) essentially correspond to the first connections, reflected along the longitudinal center axis and the transverse center axis of the semiconductor memory apparatus (14).

8. The semiconductor memory apparatus (14) as claimed in one of the preceding claims, in which the contacts (20) of the connecting apparatus (16) are in the form of a ball grid array.

9. The semiconductor memory apparatus (14) as claimed in one of the preceding claims, with the allocation device (30) comprising logic gates (42; 70).

10. The semiconductor memory apparatus (14) as claimed in one of the preceding claims, in which the contacts (20) in the second contact group (K2) are arranged essentially symmetrically with respect to the longitudinal center axis (A-A) and/or the transverse center axis (B-B) of the semiconductor memory apparatus (14).

11. The semiconductor memory apparatus (14) as claimed in one of the preceding claims, in which the signals which are to be transmitted between the internal connections (22) of the integrated semiconductor memory (18) and the contacts (20) of the connecting apparatus

(16) are not significantly changed by the transmission process.

12. A semiconductor apparatus, comprising at least two semiconductor memory apparatuses (14) as claimed in one of the preceding claims, and a printed circuit board device (12), in which

- the two semiconductor memory apparatuses (14) are arranged essentially opposite one another on opposite sides of the printed circuit board device (12), and
- the printed circuit board device (12) comprises at least one allocation supply connection (M1-M4) which can be connected to the allocation contact (44) of one semiconductor memory apparatus (14) for signaling purposes.

13. The semiconductor apparatus as claimed in claim 12, in which, during operation of the semiconductor apparatus,

- the allocation contact (44) of the first semiconductor memory apparatus (14) is not connected to the printed circuit board device (12) for signaling purposes, and the internal allocation signal (M_int; M1_int, M2_int) of the first semiconductor memory apparatus (14) assumes the first state, and
- the allocation contact (44) of the second semiconductor memory apparatus (14) is connected to a predetermined allocation supply connection (M1-M4) of the printed circuit board device (12) for signaling purposes, and the internal allocation signal (M_int; M1_int, M2_int) of the second semiconductor memory apparatus (14) assumes the second state.

14. The semiconductor apparatus as claimed in claim 13, in which the printed circuit board device (12) comprises at least two allocation supply connections (M1-M4) which

can be connected to the allocation contact of one semiconductor memory apparatus (14) for signaling purposes and, depending on the allocation supply connection (M1-M4) of the printed circuit board device (12) to which the allocation contact (44) of the second semiconductor memory apparatus (14) is connected for signaling purposes, the internal allocation signal (M_int; M1_int, M2_int) of the second semiconductor memory apparatus (14) assumes the second state or the third state.

15. The semiconductor apparatus as claimed in claim 12, in which

- the printed circuit board device (12) comprises at least four allocation supply connections (M1-M4);
- the allocation contact (44) of the first and second semiconductor memory apparatus (14) is connected to a respective predetermined allocation supply connection (M1-M4) of the printed circuit board device (12) for signaling purposes; and
- depending on the allocation supply connection (M1-M4) of the printed circuit board device (12) to which the allocation contact of the second semiconductor memory apparatus (14) is connected for signaling purposes, the internal allocation signal (M_int; M1_int, M2_int) of the second semiconductor memory apparatus (14) assumes the second state or the third state, and the internal allocation signal (M_int; M1_int, M2_int) of the first semiconductor memory apparatus (14) assumes the first state or the fourth state.